REMARKS/ARGUMENTS

This case has been carefully reviewed and analyzed in view of the final Official Action dated 5 January 2005. Responsive to the rejections made by the Examiner in the Official Action, Claims 1, 6, 11, 13, 16 and 17 have been amended and are now believed to be clearer in their respective recitations. Claims 1, 3, 5 – 7, 9, 11 – 14 and 16 – 18 will be pending in this Application upon entry of this Amendment.

In the Official Action, the Examiner rejected Claims 1, 3, 5 – 7, 9, 11 – 14 and 16 – 18 under 35 U.S.C. § 102(e) as being anticipated by Gafken, et al. (U.S. Patent # 6,157,970; hereinafter "Gafken"). In setting forth the rejections, the Examiner cited the single LPC bus of the reference as fulfilling the claimed limitations of "a first LPC bus..." and "a second LPC bus...". The Examiner further cited the LPC bus signal lines LAD[3:0] as fulfilling the claimed "address register for storing a target address".

The invention of the subject Patent Application, by virtue of its beneficial features, overcomes certain shortcomings of traditional implementations of the LPC bus. As Applicant's Claims now more clearly recite, the subject invention includes "an LPC host controller including an address register for storing a target address". When installed across separated LPC buses, communication between LPC devices on the separate buses may be conducted since, among other things, "said LPC host controller [is] further operable to initiate concurrently a first access

cycle on said first LPC bus and a second bus access cycle on said second LPC bus". When installed on a single bus, for example, the communication may be carried out because, in addition to other features, "said LPC host controller [is] operable to initiate a data transfer cycle on said LPC bus, said data transfer cycle being a concatenation of a first bus access cycle for LPC bus access by [a] master LPC device and a second bus access cycle for LPC bus access by [a] ... slave LPC device".

The full combination of these and other beneficial features now more clearly recited by Applicant's pending Claims are nowhere disclosed, suggested or even alluded to in Gafken. At the outset, it is respectfully submitted that the Examiners assertions that the claimed "a first LPC bus..." and "a second LPC bus..." are met by the **single** bus of the reference are unfounded. It should be clear from the claim language, which is in accordance with accepted Patent practice, that the claimed "first LPC bus" and "second LPC bus", when taken in conjunction with a reading of the Specification, are **not** the same bus. However, the Examiner's rejections are based, in part, on the reasoning that the claimed "first LPC bus" and "second LPC bus" are met by bus 124 of Gafken. It is thus submitted, respectfully, that such rejections are improper and should be withdrawn.

In the Official Action, the Examiner alleged that the reference shows the claimed "LPC host controller ... operable to initiate a first bus access cycle on said

first LPC bus and a second bus access cycle on said second LPC bus...", although the location in the reference of such teaching was neither given by the Examiner nor established by the Applicant. However, in column 5, lines 2 – 20 of Gafken, it is clearly stated that the assertion of LFRAME# on the single LPC bus during an LPC transaction aborts any transaction on the bus. This makes clear that, in Gafken, any bus access cycle initiated by the assertion of LFRAME# would terminate any bus activity associated with a previously established bus access cycle. Gafken, then, **clearly teaches away** from an "LPC host controller ... operable to initiate concurrently a first bus access cycle on said first LPC bus and a second bus access cycle on said second LPC bus...", as is now claimed in the subject Patent Application, since, on the **single** LPC bus described in the reference, only a single bus access cycle is allowed at any instance of time.

As previously stated, the Examiner cited Gafken as disclosing an address register in the LPC host controller by referring to the address lines LAD[3:0]. Admittedly, the bus control logic of Gafken includes a buffer and may have temporary storage of data that is output on LAD[3:0], but there is no indication in Gafken that a target address is stored in an address register located at any LPC device, especially since during any clock cycle, only a few bits corresponding to a partial address are allowed to be transmitted over the bus. Perhaps the Examiner is inferring some other hardware associated with the signal lines LAD[3:0], but it is respectfully submitted that rejecting the limitation of "an address register" by

citing signal lines is not sufficient in making that inference known. In fact, it is unclear to Applicant how many of the passages cited by the Examiner are relevant to the claimed limitations they allegedly disclose and clarification is respectfully requested should there be any further rejections following this Amendment.

The invention of the subject Patent Application includes "an LPC host controller ... operable to initiate concurrently a first bus access cycle on said first LPC bus and a second bus access cycle on said second LPC bus", as amended Claim 1 now more clearly recites. In complementary fashion, amended Claim 6 recites "initiating a second bus access cycle on said second LPC bus by said LPC host controller concurrently while said first LPC bus is in [a] wait state". Neither of these are disclosed or suggested by Gafken and, as such, the invention so claimed is neither anticipated by nor made obvious by the reference. Additionally, amended Claim 11 recites the limitation of "an address register operable to persistently store a target address" and, similarly, amended Claim 13 recites the limitation of "providing ... an address register operable to store a target address persistently over at least two bus access cycles on an LPC bus". These limitations in combination with the other limitations recited are also not disclosed or suggested by the Gafken and the invention so claimed cannot be anticipated or made obvious by the reference.

It is now believed that the independent Claims of the subject Patent Application, as now amended, are allowable over the prior art of record. That

being so, it is further believed that the dependent Claims are allowable for at least the same reasons for which the corresponding independent Claim from which they are respectively dependent are allowable.

The remaining references cited by the Examiner, but not used in the rejections, have been reviewed, but are believed to be further remote from the subject Patent Application than the reference cited by the Examiner when patentable considerations are taken into account.

It is now believed that the subject Patent Application has been placed in condition for allowance and such action is respectfully requested.

Respectfully submitted
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